

ABSTRACT OF THE DISCLOSURE

A decoder for decreasing the load on a microcomputer. The decoder stores in a buffer memory in sector units
5 digital data. The decoder includes a check head register for storing a first address of the buffer memory when storing the processed digital data in the buffer memory. A check sector counter counts the number of sectors of the processed digital data stored in the buffer memory to generate a count
10 value. A command decision circuit decides whether digital data requested to be transferred is stored in the buffer memory based on the first address, the count value, and a head address of the digital data. The command decision circuit permits the decoder to transfer the processed
15 digital data when deciding that the digital data requested to be transferred is stored in the buffer memory.